

Product Features

- Electrical interface specifications per SFF-8431
- Management interface specifications per SFF-8431 and SFF-8472
- SFP+ MSA package with Single LC receptacle
- 1490nm EML Laser, APD photo-detector
- Up to 11.3G bi-directional data links
- Single +3.3V power supply
- Class 1 laser safety certified
- Operating temperature Options
 - (Commercial) 0°C to +70°C
 - (Industrial) -40°C to +85°C
- Up to 80km on 9/125µm SMF
- RoHS6 Compliant



Applications

- 10GBASE-BX Ethernet
- 10GBASE-ZR at 10.3125Gbps
- 10GBASE-ZW at 9.953Gbps
- CPRI 2/3/4/5/6/7/8 and OBSAI 2X/4X/8X

Descriptions

LX4441C(I)DR are designed for Single Fiber Bidirectional serial optical data communications up to 11.3 Gb/s. The electrical interface is compliant with SFI specifications of SFF-8431. The transceiver consists of 10Gbit/s 1490nm EML optical transmitter and APD receiver, and transmission distance up to 80Km on single mode fiber.

LX4441C(I)DR offer commercial and industrial operating temperature options.

Ordering Information

Table 1. Ordering Information

Part Number	Transmitter	Output Power	Receiver	Sensitivity	Reach	Temp	DDM	RoHS
LX4441CDR	1490nm EML	+0 ~ +4dBm	1550nm APD	< -24dBm	80km	0 ~ 70 °C	Available	Compliant
LX4441IDR	1490nm EML	+0 ~ +4dBm	1550nm APD	< -24dBm	80km	-40 ~ 85 °C	Available	Compliant

Pin Description

Table 2. Pin Description

Pin	Name	Function/Description	Notes
1	VeeT	Transmitter Ground	1

2	TX_Fault	Transmitter Fault (LVTTTL-O) - High indicates a fault condition	2
3	TX_Disable	Transmitter Disable (LVTTTL-I) – High or open disables the transmitter	3
4	SDA	Two wire serial interface Data Line (LVCMOS-I/O) (MOD-DEF2)	4
5	SCL	Two wire serial interface Clock Line (LVCMOS-I/O) (MOD-DEF1)	4
6	MOD_ABS	Module Absent (Output), connected to VeeT or VeeR in the module	5
7	RS0	Internal 33KΩ pull-down to ground	-
8	RX_LOS	Receiver Loss of Signal (LVTTTL-O)	2
9	RS1	Internal 33KΩ pull-down to ground	-
10	VeeR	Receiver Ground	1
11	VeeR	Receiver Ground	1
12	RD-	Inverse Received Data out (CML-O)	-
13	RD+	Received Data out (CML-O)	-
14	VeeR	Receiver Ground	-
15	VccR	Receiver Power - +3.3V	-
16	VccT	Transmitter Power - +3.3 V	-
17	VeeT	Transmitter Ground	1
18	TD+	Transmitter Data In (CML-I)	-
19	TD-	Inverse Transmitter Data In (CML-I)	-
20	VeeT	Transmitter Ground	1

Notes:

1. The module signal grounds are isolated from the module case.
2. This is an open collector/drain output that on the host board requires a 4.7KΩ to 10KΩ pull-up resistor to VccHost.
3. This input is internally biased high with a 4.7KΩ to 10KΩ pull-up resistor to VccT.
4. Two-Wire Serial interface clock and data lines require an external pull-up resistor dependent on the capacitance load.
5. This is a ground return that on the host board requires a 4.7KΩ to 10KΩ pull-up resistor to VccHost.

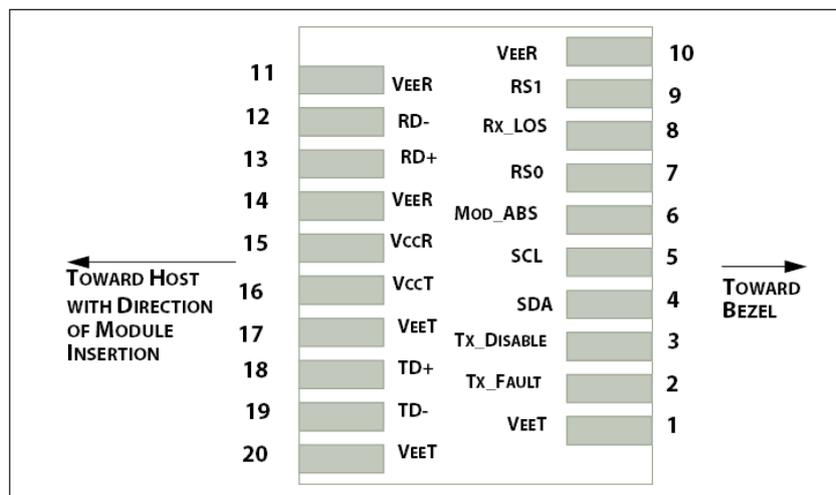


Figure 1. Host PCB SFP+ pad assignment top view

Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

Table 3. Absolute Maximum Ratings

Parameter	Symbol	Minimum	Maximum	Unit
Storage Temperature	T _s	-40	85	°C
Relative Humidity	RH	5	95	%
Supply Voltage	V _{CC}	-0.3	4.0	V

Recommended Operating Conditions

Table 4. Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	
Operating Case Temperature	LX4441CDR	T _C	0	25	70	°C
	LX4441IDR	T _C	-40	25	85	°C
Supply Voltage	V _{CC}	3.135	3.3	3.465	V	
Data Rate	-	1	9.95 10.3	11.3	Gb/s	

Transceiver Electrical Characteristics

Table 5. Transceiver Electrical Characteristics

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Notes	
Module Supply Current(C-Temp)	I _{CC}	-	-	450	mA	-	
Power Dissipation(C-Temp)	P _D	-	-	1500	mW	-	
Module Supply Current(I-Temp)	I _{CC}	-	-	550	mA	-	
Power Dissipation(I-Temp)	P _D	-	-	1800	mW	-	
Transmitter							
Input Differential Impedance	Z _{IN}	-	100	-	Ω	-	
Differential Data Input Swing	V _{IN, P-P}	180	-	700	mV _{P-P}	-	
TX_FAULT	Transmitter Fault	V _{OH}	2.0	-	V _{CCHOST}	V	-
	Normal Operation	V _{OL}	0	-	0.8	V	-
TX_DISABLE	Transmitter Disable	V _{IH}	2.0	-	V _{CCHOST}	V	-
	Transmitter Enable	V _{IL}	0	-	0.8	V	-
Receiver							

Output Differential Impedance	Z_o	-	100	-	Ω	-	
Differential Data Output Swing	$V_{OUT, P-P}$	400	-	850	mV _{P-P}	1	
Data Output Rise Time, Fall Time	t_r, t_f		-	60	ps	2	
RX_LOS	Loss of signal (LOS)	V_{OH}	2.0	-	V_{CCHOST}	V	3
	Normal Operation	V_{OL}	0	-	0.8	V	3

Notes:

1. Internally AC coupled, but requires a external 100 Ω differential load termination.
2. 20–80%.
3. LOS is an open collector output. Should be pulled up with 4.7k Ω on the host board.

Transmitter Optical Characteristics

Table 6. Transmitter Optical Characteristics

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Notes
Launch Optical Power	P_o	+0	-	+4	dBm	1
Center Wavelength Range	λ_c	1480	1490	1500	nm	-
Extinction Ratio	EX	8.2	-	-	dB	2
Spectral Width (-20dB)	$\Delta\lambda$	-	-	1	nm	-
Side Mode Suppression Ratio	SMSR	30	-	-	dB	-
Relative Intensity Noise	RIN			-128	dB/Hz	
Pout @TX-Disable Asserted	P_{off}	-	-	-35	dBm	1

Notes:

1. The optical power is launched into 9/125 μ m SMF.
2. Measured with a PRBS 2³¹-1 test pattern @ 10.3125Gbps.

Receiver Optical Characteristics

Table 7. Receiver Optical Characteristics

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Notes
Center Wavelength	λ_c	1540	1550	1560	nm	-
Receiver Sensitivity (P_{avg})	S1	-	-	-24	dBm	1
Receiver Sensitivity (P_{avg})@80km	S2	-	-	-21	dBm	1
Receiver Overload (P_{avg})	P_{OL}	-7	-	-	dBm	1
Optical Return Loss	ORL	27	-	-	dB	-
LOS De-Assert	LOS_D	-	-	-25	dBm	-
LOS Assert	LOS_A	-35	-	-	dBm	-
LOS Hysteresis	-	0.5	-	-	dB	-

Notes:

1. Measured with PRBS 2³¹-1 test pattern, 10.3125Gb/s, BER<10⁻¹².

Recommended Host Board Power Supply Filter Network

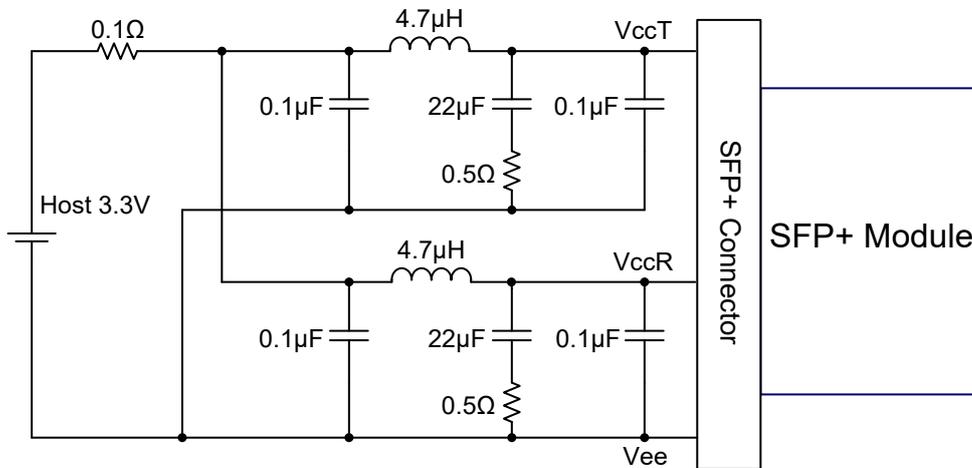


Figure 2. Recommended Host Board Power Supply Filter Network

Recommended Application Interface Block Diagram

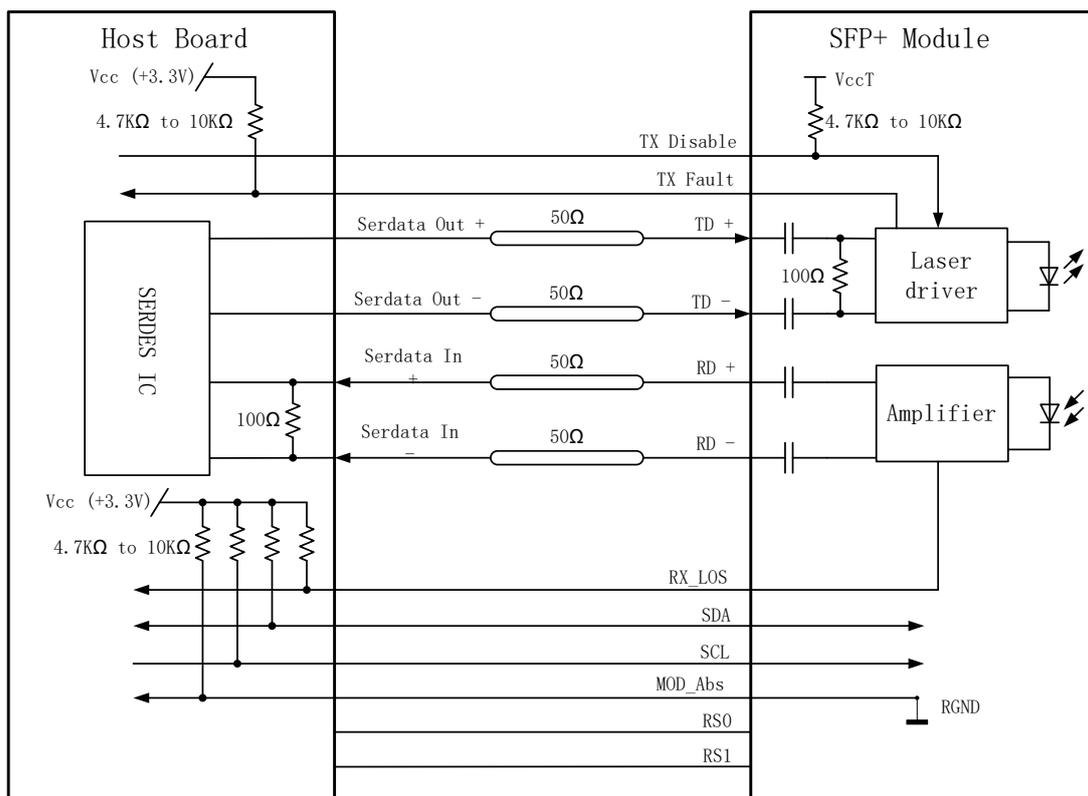


Figure 4. Recommended Application Interface Block Diagram

Mechanical specifications

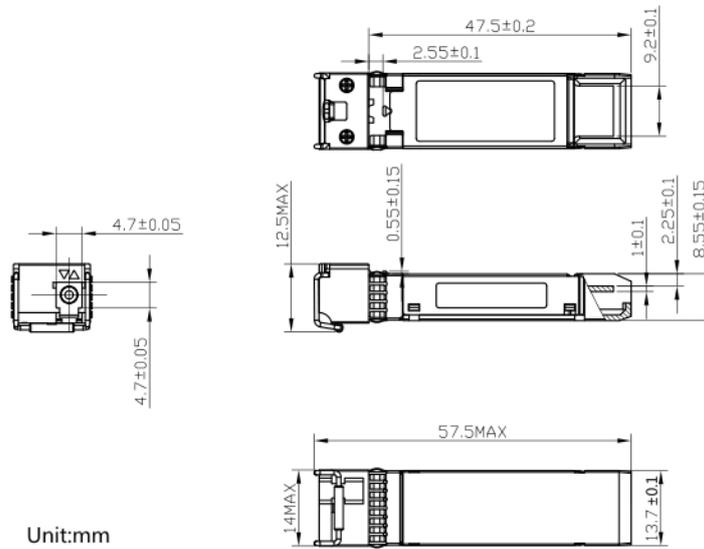
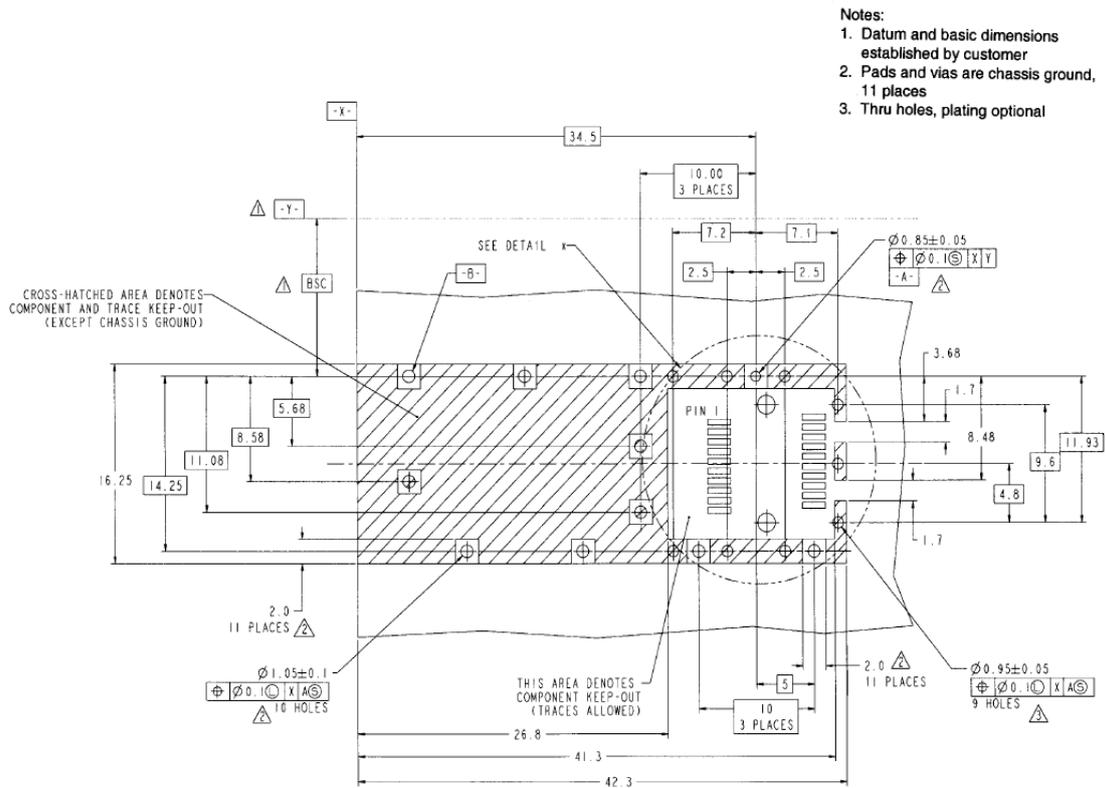


Figure 5. Outline Drawing

PCB layout recommendation



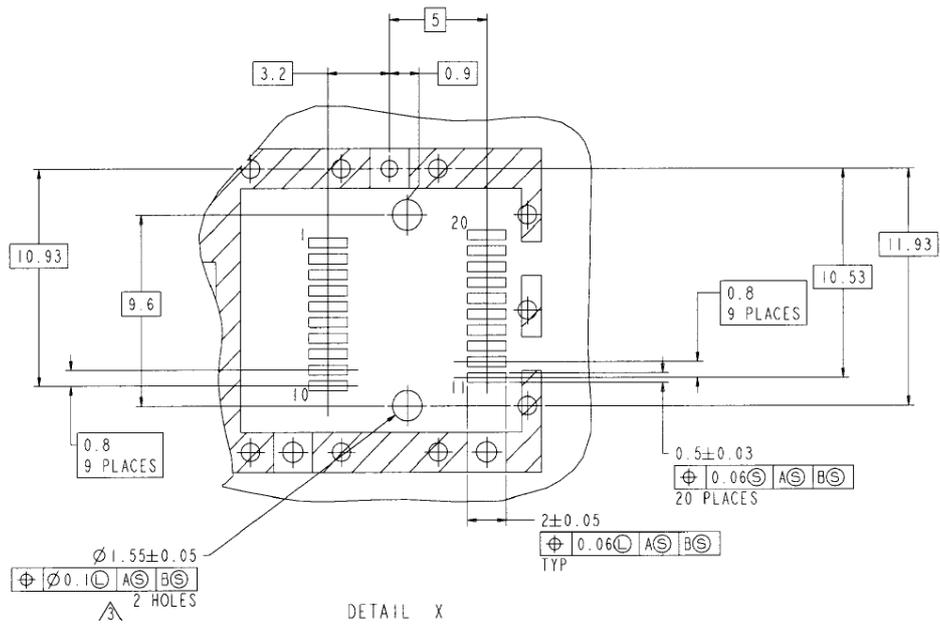


Figure 6. PCB layout recommendation

Revision History

Revision	Revision History	Release Date
1.0	Released	Nov. 4, 2019
1.1	Receiver Sensitivity (P_{avg})@80km updated	Nov. 27, 2019
1.2	Adjust Receiver Sensitivity (P_{avg}) from -23 to -24dBm; Adjust Receiver Sensitivity (P_{avg})@80km from -20 to -21dBm	Nov. 21, 2020

For More Information

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