

Product Features

- Up to 25.78Gb/s bi-directional data links
- Electrical interface specifications per SFF-8431
- Management interface specifications per SFF-8432 and SFF-8472
- Build-in CDR with shut off control
- SFP+ MSA package with duplex LC connector
- Uncooled 850nm VCSEL Laser
- Single +3.3V power supply
- Class 1 laser safety certified
- Metal enclosure, for lower EMI
- Commercial operating temperature: 0°C to +70°C
- Up to 70m on OM3 MMF and 100m on OM4 MMF
- RoHS Compliant



Applications

- 25.78Gb/s single lane 100GE SR4

Descriptions

LX6501CDH SFP28 transceivers, according to 25Gigabit Small Form Factor Pluggable “SFP28” Multi-Sourcing Agreement (MSA) SFF-8431 Rev. 4.1 and SFF-8472 Rev. 12.1, are designed for use up to 25.78Gb/s data rate over multimode fiber. They are compatible with SFF-8432.

LX6501CDH offer commercial operating temperature option.

Ordering Information

Table 1. Ordering Information

Part Number	Transmitter	Output Power	Receiver	Sensitivity	Reach	Temp	DDM	RoHS
LX6501CDH	850nm VCSEL	-7.6 ~ +2.4dBm	PIN	<-11dBm	70m	0 ~ 70°C	Available	Compliant

Pin Description

Table 2. Pin Description

Pin	Name	Function/Description	Notes
1	VeeT	Transmitter Ground	1
2	TX_Fault	Transmitter Fault (LVTTTL-O) - High indicates a fault condition	2

3	TX_Disable	Transmitter Disable (LVTTL-I) – High or open disables the transmitter	3
4	SDA	Two wire serial interface Data Line (LVCMOS-I/O) (MOD-DEF2)	4
5	SCL	Two wire serial interface Clock Line (LVCMOS-I/O) (MOD-DEF1)	4
6	MOD_ABS	Module Absent (Output), connected to VeeT or VeeR in the module	5
7	RS0	Rate Select 0 – Not used, Presents high input impedance	6
8	RX_LOS	Receiver Loss of Signal (LVTTL-O)	2
9	RS1	Rate Select 1 – Not used, Presents high input impedance	6
10	VeeR	Receiver Ground	1
11	VeeR	Receiver Ground	1
12	RD-	Inverse Received Data out (CML-O), AC Coupled	-
13	RD+	Received Data out (CML-O), AC Coupled	-
14	VeeR	Receiver Ground	-
15	VccR	Receiver Power - +3.3V	-
16	VccT	Transmitter Power - +3.3 V	-
17	VeeT	Transmitter Ground	1
18	TD+	Transmitter Data In (CML-I), AC Coupled	-
19	TD-	Inverse Transmitter Data In (CML-I), AC Coupled	-
20	VeeT	Transmitter Ground	1

Notes:

1. The module signal grounds are isolated from the module case.
2. This is an open collector/drain output that on the host board requires a 4.7KΩ to 10KΩ pull-up resistor to VccHost.
3. This input is internally biased high with a 4.7KΩ to 10KΩ pull-up resistor to VccT.
4. Two-Wire Serial interface clock and data lines require an external pull-up resistor dependent on the capacitance load.
5. This is a ground return that on the host board requires a 4.7KΩ to 10KΩ pull-up resistor to VccHost.
6. Rate select can also be set through the 2-wire bus in accordance with SFF-8472 v. 10.2, Rx Rate Select is set at Bit 3, Byte 110, Address A2h. Tx Rate Select is set at Bit 3, Byte 118, Address A2h.

Note: writing a “1” selects maximum bandwidth operation. Rate select is the logic OR of the input state of Rate Select Pin and 2-wire bus.

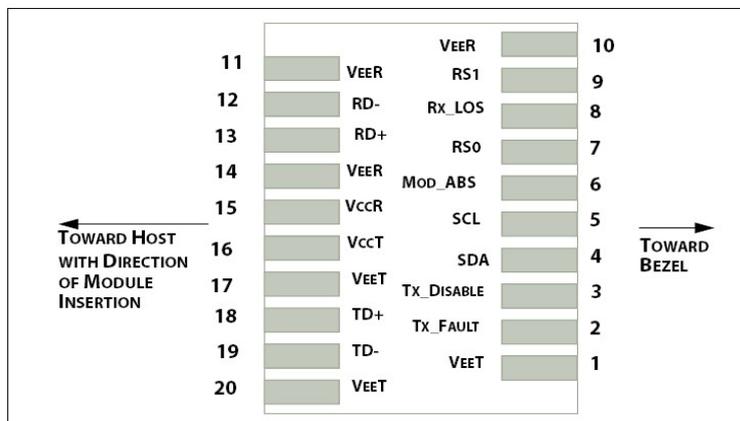


Figure 1. Host PCB SFP+ pad assignment top view

Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

Table 3. Absolute Maximum Ratings

Parameter	Symbol	Minimum	Maximum	Unit
Storage Temperature	T _s	-40	85	°C
Relative Humidity	RH	5	95	%
Supply Voltage	V _{cc}	-0.5	4.0	V

Recommended Operating Conditions

Table 4. Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Operating Case Temperature	T _c	0	25	70	°C
Supply Voltage	V _{cc}	3.135	3.3	3.465	V
Data Rate	-	-	25.78	-	Gb/s

Transceiver Electrical Characteristics

Table 5. Transceiver Electrical Characteristics

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Notes	
Module Supply Current	I _{cc}	-	-	290	mA	-	
Power Dissipation	P _D	-	-	1000	mW	-	
Transmitter							
Input Differential Impedance	Z _{IN}	-	100	-	Ω	-	
Differential Data Input Swing	V _{IN, P-P}	180	-	700	mV _{P-P}	-	
TX_FAULT	Transmitter Fault	V _{OH}	2.0	-	V _{cc}	V	TX_FAULT
	Normal Operation	V _{OL}	0	-	0.8	V	
TX_DISABLE	Transmitter Disable	V _{IH}	2.0	-	V _{cc}	V	TX_DISABLE
	Transmitter Enable	V _{IL}	0	-	0.8	V	
Receiver							
Output Differential Impedance	Z _O	-	100	-	Ω	-	
Differential Data Output Swing	V _{OUT, P-P}	300	-	850	mV _{P-P}	1	
Data Output Rise Time, Fall Time	t _r , t _f	-	30	-	ps	2	
RX_LOS	Loss of signal (LOS)	V _{OH}	2.0	-	V _{cc}	V	RX_LOS
	Normal Operation	V _{OL}	0	-	0.8	V	

Notes:

- Internally AC coupled, but requires a external 100Ω differential load termination.

2. 20–80%.
3. LOS is an open collector output. Should be pulled up with 4.7KΩ on the host board.

Transmitter Optical Characteristics

Table 6. Transmitter Optical Characteristics

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Notes
Launch Optical Power	P _o	-7.6	-	+2.4	dBm	1
Extinction Ratio	ER	2	-	-	dB	
Center Wavelength Range	λ _c	840	850	860	nm	-
Transmitter Dispersion Penalty @25.78Gb/s	TWDP	-	-	5	dB	
Spectral Width (RMS) @25.78Gb/s	Δλ	-	-	0.6	nm	-
Optical Return Loss Tolerance	ORLT	-	-	12	dB	-
P _{out} @TX-Disable Asserted	P _{off}	-	-	-30	dBm	1

Notes:

1. 50/125μm fiber with NA = 0.2, 62.5/125μm fiber with NA = 0.275.

Receiver Optical Characteristics

Tale 7. Receiver Optical Characteristics

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Notes
Center Wavelength	λ _c	840	-	860	nm	-
Receiver Sensitivity (P _{avg})	S	-	-	-11	dBm	1
Receiver Overload (P _{avg})	P _{OL}	2.5	-	-	dBm	
Optical Return Loss	ORL	12	-	-	dB	-
LOS De-Assert	LOS _D	-	-	-12	dBm	-
LOS Assert	LOS _A	-30	-	-	dBm	-
LOS Hysteresis	-	0.5	-	-	dB	-

Notes:

1. Measured with PRBS 2³¹-1 at 10⁻⁴ BER @25.78Gb/s.

Recommended Host Board Power Supply Filter Network

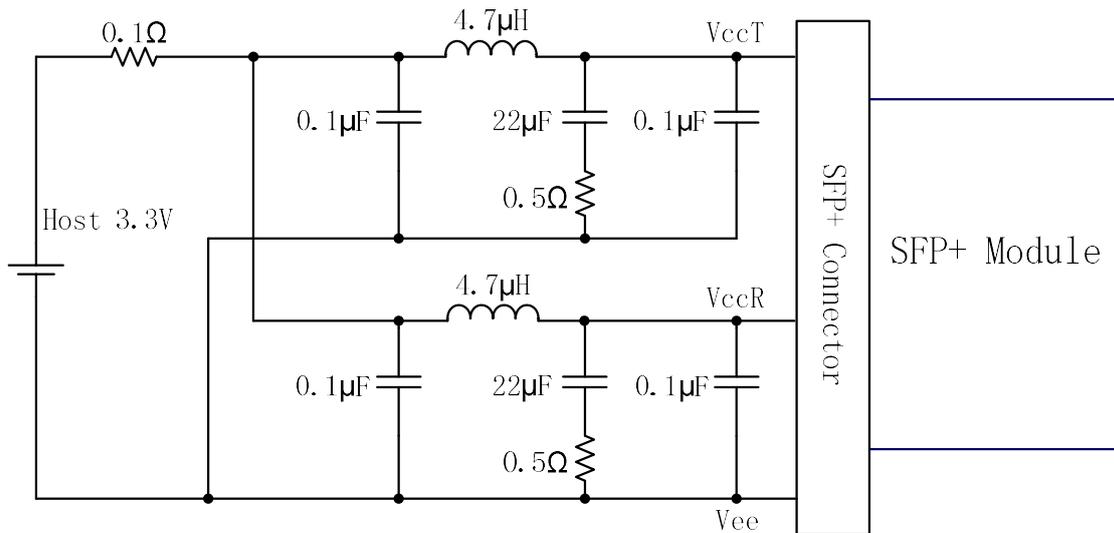


Figure 2. Recommended Host Board Power Supply Filter Network

Recommended Application Interface Block Diagram

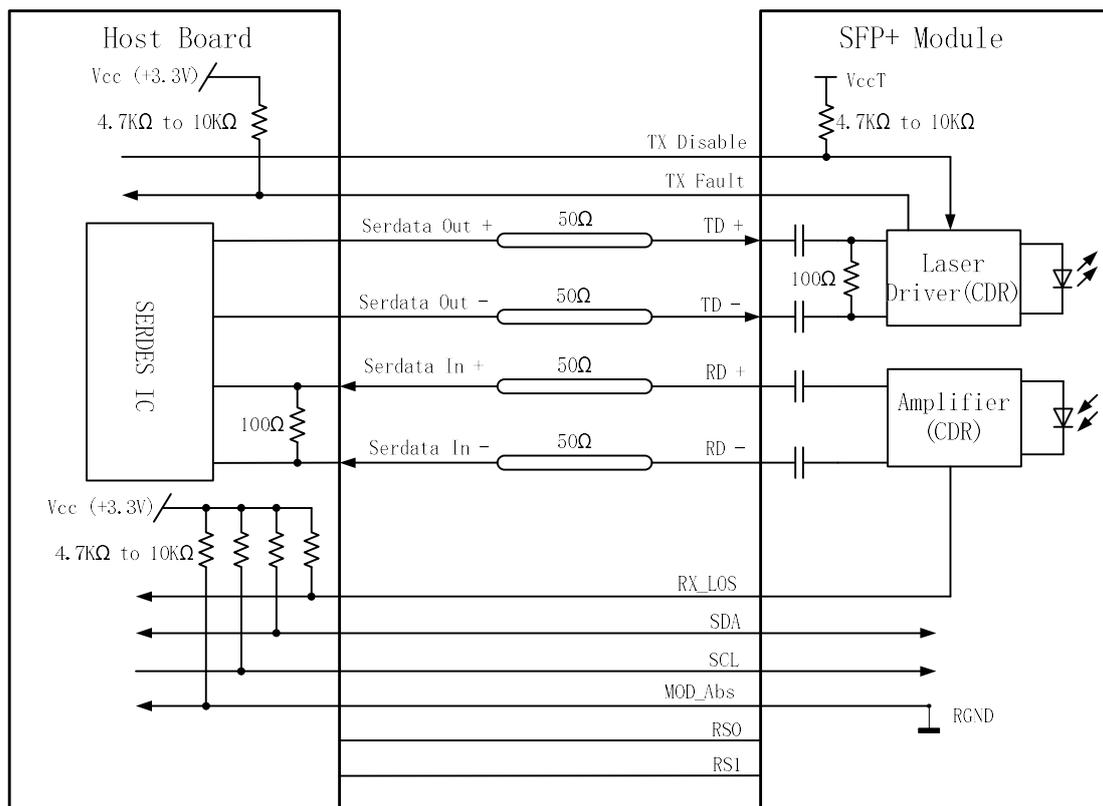


Figure 3. Recommended Application Interface Block Diagram

Mechanical specifications

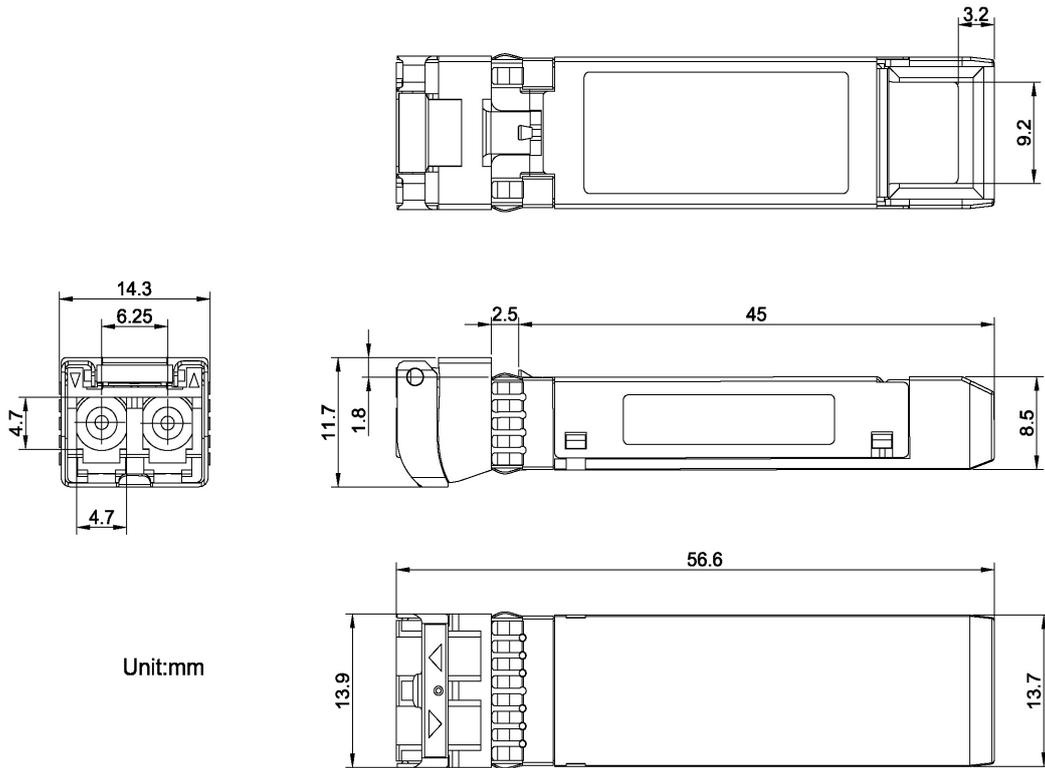


Figure 4. Outline Drawing

PCB layout recommendation

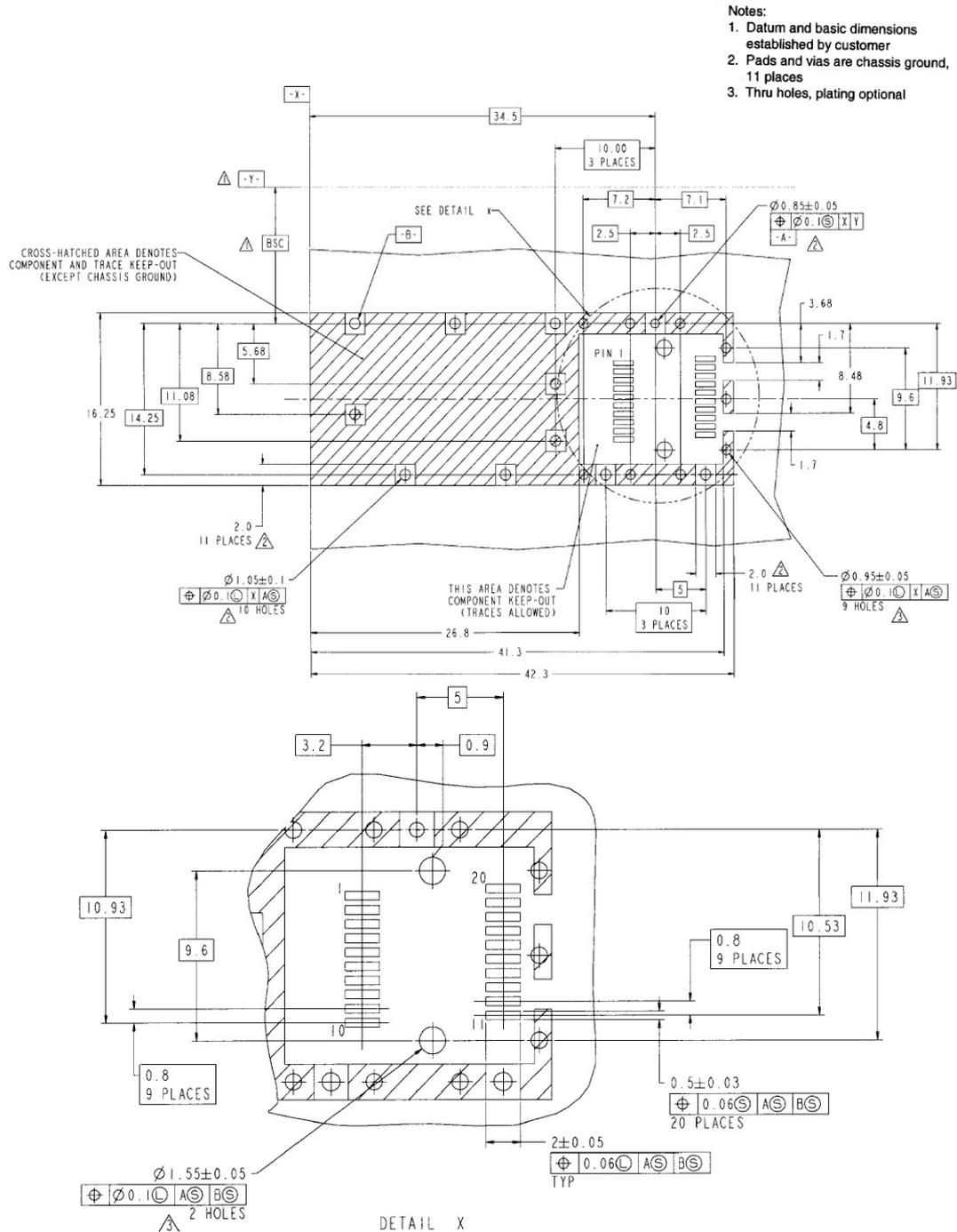


Figure 5. PCB layout recommendation

For More Information

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